A novel technique of Quadruple-Source/Drain (4-Output) & Multi-Gate (Input) Relay Design

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Abstract - This paper focuses on robust technique for Quadruple-Source/Drain and Multi –Gate relay designs. Logic gate designs unique to relays can be achieved by taking advantage of the electrostatic force dependence on the actuation electrode area [6], [7]. For example, by carefully designing the beam dimensions, the number of driving input electrodes required to actuate a relay can be adjusted to implement two-input AND, OR [7], and NAND [6] gates. This design technique can be extended to other types of logic gates. This concept can be applied to the relay design in this paper. The fixed electrode (used as gate) can be subdivided into multiple separate electrodes that can be independently biased. This way, the strength of electrostatic force (therefore actuation) can be controlled by the number of input electrodes (gate) that are driven.

Index Terms— actuation, beam, electrode, drain, Quadruple, relays.

I. QUADRUPLE-SOURCE/DRAIN (4-OUTPUT) RELAY DESIGN

The concept of multiple-source/drain can be extended to relays with >2 source/drain pairs. As proof of concept, a quadruple-source/drain (4-output) relay is fabricated in real terms (Figure 1) (1). Functionality is verified by measured ID-VG curves shown in Figure 2. Each drain is biased at different voltage levels to achieve different current levels. Actuation is found to be symmetric as switching voltages for all four source/drain pairs coincide. Note that symmetric switching is only achieved when the actuation plate is flat, stressing the increased importance of low strain gradient material for multisource/drain designs. (1)

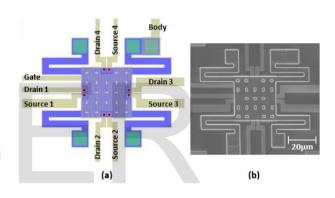


Fig 1: Illustrations of a quadruple-source/drain relay structure (1). (a) Layout view indicating the terminals. (b) Top-view scanning electron micrograph (SEM) image.

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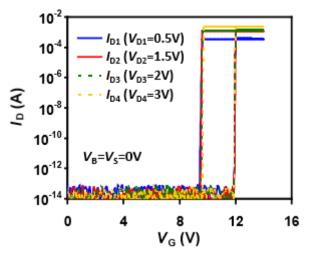


Fig 2: Measured IDS-VG characteristics of a quadruplesource/drain relay. Different current levels are seen, corresponding to different applied VD's.

II. MULTI-GATE (INPUT) RELAY

For a given process technology, there are several ways to design the relay to implement different logic functions:

- (1) Subdivision of the fixed electrode: Since electrostatic force depends on the total actuating electrode area, the fixed electrode can be replaced with smaller electrodes of equal area to accommodate multiple inputs - or of different areas to accommodate multiple inputs of varying weight (i.e. influence) - to implement different logic functions.
- (2) Relay dimensions: The flexure and plate dimensions determine the total electrostatic force needed to turn on the relay. For example, by adjusting flexure length (i.e. stiffness), a relay can be made to turn on with either one or two driven inputs.
- (3) Body biasing: Given a certain input voltage range, relays can be set to turn on when a specific numbers of input electrodes is driven by appropriately setting the level of body bias. In this manner, the same relay structure can be used to achieve different logic functions.

A possible drawback of the multi-input approach is scalability. When the fixed electrode is subdivided, there is a minimum separation distance between the electrodes. This distance is limited by surface leakage. In this work, the separation distance between electrodes is > 0.5 μ m. As the size of the relay is scaled down, the amount of fixed electrode area lost due to electrode-to-electrode separation becomes a larger portion of the total area. As a result, actuation becomes less effective. Despite limited scalability, multi electrode design potentially enables any logic function to be implemented with only two relays.

Therefore, overall area savings can be achieved from a system standpoint. In this work, dual-gate (2-input) relays are demonstrated. This concept can be extended to relays with >2 input electrodes [8].

III. DUAL GATE 2-INPUT RELAY DESIGN

The fabricated dual-gate (2-input), dualsource/drain (2-output) relay structure is shown in Figure 3. Note that the gate electrodes have equal area and are inter-digitated to ensure that they have equal influence (1). In addition to this, Figure 4 shows VPI and VRL of the dual-gate relay when VB = 0 V. The first case, [0,1], is when only Gate 2 is driven, and the second case, [1,0], is when only Gate 1 is driven. The non-driven gate is kept at 0 V. Switching voltages are equal for both cases, confirming Gate 1 and 2 have equal influence. The third case, [1,1], is when both gates are driven simultaneously to actuate the relay. As expected, the switching voltages are lower in this case due to stronger electrostatic force for the same voltage since the effective actuation area is doubled in this case. With this property, different levels of body bias can be applied to make the relay switch using either one gate or two gate electrodes for the same voltage.(1) For example, an operating voltage of 12 V requires both gates to be driven to turn the relay on with VB = 0 V (AND When VB = -5 V is applied, the function). switching voltages are lowered, so that driving just one of the gates is sufficient to turn the relay on (OR function). In Figure 4, body biasing requirements to achieve AND and OR function are indicated for VG = 8 V.

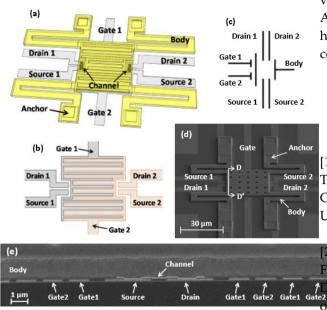


Fig 3: Schematic views of a dual-gate, dualsource/drain relay. (a) Isometric view. (b) Bottom electrode layout (c) Circuit symbol. (d) Scanning electron micrograph (SEM) image of a dual-gate, dualsource/drain relay. (e) Cross-sectional SEM from focused ion beam (FIB) cut at D-D'.

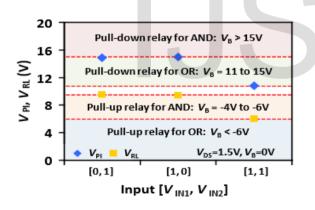


Fig 4: Measured pull-in (VPI) and release (VRL) voltages of a dual-gate relay, for various input combinations

III CONCLUSION

In this paper, a novel design technique of Quadruple-Source/Drain (4-Output) & Multi-Gate (Input) Relay Design has been given. Results computed show that a sharp change in pull in voltage (VPI) and release voltage (VRL) is observed as compared to other designs. Also the quadruple source-drain relay design presented here is expected to be more robust and coherent as compared to its counterparts.

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